

Gordon G Seagrave
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(202) 253-5517

Patents:

United States Patent 2007: Patent No.: 7,249,153 B2, entitled "Data Compression Using Cbeyshev Transform"

Patent Pending : SpaceCube

Awards:

NASA ONE Award - 2006

NASA Exceptional Achievement Award - 2007

Publications:

"CRISM Scan System"

Kim Strohhahn, Teck Choo, John Hayes ,Gene Heyler, Jeff Lees, Dave Lohr, Gordon Seagrave
X-Ray, UV, Visible, and IR Instrumentation for Planetary Missions, September 2009

"Universal Reconfigurable Processing Platform for Space"

D. SEAGRAVE, G. SEAGRAVE

MAPLD Conference, Annapolis MD., September 2009

"SpaceCube : A Reconfigurable Computing Hardware Platform for Space Applications"

G. SEAGRAVE, D. SEAGRAVE, J. GODFREY, M. LIN,

MAPLD Conference, Annapolis MD., September 2008

"Implementations of two motion detectors: Shunting and Reichardt".

G. SEAGRAVE, B.NABET, V.SHREESHA, L.LOELILO, F.YOUNG, A.LEUYTSKY

Proceedings Network for Learning Recognition and Control,
WANG Institute of Boston University, p.66 May 14-16 1992

"Elements of an on chip visual system".

B. NABET, G.SEAGRAVE, L.HOJDA AND A.SCOLES

Proceedings Network of Vision and Image Processing,
WANG Institute of Boston University, p.46 May 10-12 1991

Education:

Drexel University

BS, Electrical and Computer Engineering- Degree 1992

Technical Summary:

Languages: VHDL, AHDL, VERILOG, C, BASIC, PASCAL, Assembly

Hardware: LEON3FT UT699, Aeroflex 6325, ACTEL RTAX2000, ACTEL RT54SX72A, ALTERA CYCLONE, ALTRA 10K100, Xilinx Virtex 4, Xilinx Virtex XCV300E, Xilinx 4028, Xilinx 4k, TMS320c3x, TMS320c5x, Intel 805x, Motorola 68k, PCI

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Employment Experience:

StarVision Technologies, inc (1/10 – Present)

Position: *Designer*

- Reconfigurable Space Flight DSP Board
 - Xilinx Virtex4 for Space Flight
 - Schematic Orcad
 - Power Supply Design

AEROFLEX / GORDONICUS LLC (2009 – 2010)

Position: Principal Investigator

- Reconfigurable Space Flight Processor Board
 - Xilinx Virtex4 for Space Flight
 - LEON3FT UT699 Aeroflex
 - Self Checking Testbench
 - cPCI
 - 8 port SpaceWire router
 - 3U cPCI design

SatCon Applied Technology (5/09 – 12/09)

Position: *Designer*

- DSP controlled Power Electronics IGBT Driver Board for 3-Phase UPS
 - TMS320F2812 DSP
 - Altera Cyclone III
 - Orcad Schematic

ORBITAL SCIENCES CORPORATION (2/08 – 7/09)

Position: *Scientist*

- COTS Program:
 - Board Lead for Bulk Memory Module
 - Self Checking Testbench
 - RTAX FPGA
 - 1553
 - SDRAM Controller with Reed Solomon EDAC
 - FLASH Controller
 - cPCI
- IRAD LeoStar3
 - Orbital next generation bus architecture

Position: *Senior Principle Engineer* (2/04 – 5/05)

- AIM Satellite:
 - Designed Serial Interface to Fiber Optic Gyro
 - Modified Heritage Microcontroller Board ACTEL RT54SX32A to Accommodate new Commands
- IR&D ASIC Trade Study for RAD-HARD Space FPGAs and ASICs

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ORBITAL SCIENCES CORPORATION CONT. (10/99 – 10/01)

Position: *Senior Principle Engineer*

- Panamsat Satellite:
 - Designed SDLC Interface For Uplink ACTEL RT54SX32A
 - Designed Downlink Interface ACTEL RT54SX32A
- OrbView4 Satellite: Designed Interface to Fiber Optic Gyro with ACTEL 14100
- N-STAR Satellite:
 - ACTEL RT54SX32 FPGA and board design for Propulsion Card,
 - ACTEL RT54SX32 FPGA and board design for Switch Card,
 - ACTEL RT54SX32 FPGA Sensor Cards
- QUIKToms Satellite:
 - Developed two FPGAs for Mission Interface Unit.
 - ACTEL 14100, ALTRA 10K30.

GODDARD SPACE FLIGHT CENTER (NASA) (5/05 – 1/08)

Position: *Chief Architect / Gate Array Lead / Inventor of SpaceCube*

- IR&D SpaceCube – 4in x 4in reconfigurable space based super computer
 - Xilinx Virtex4 and AeroFlex 6325 implementation
 - Designed, built and tested hardware prototype
 - Leadership role in development from idea to flight design
 - Guided software development

Position: *Senior Engineer*

- Lunar Reconnaissance Orbiter:
 - Implemented I2C (VHDL) inter board communication scheme
 - Designed Communications board
 - Designed GSE for Communications board

Position: *Lead Engineer*

- Hubble Repair Vehicle (HRV) :
 - KuBand Card
 - Designed Xilinx board for reconfigurable space based computing architecture

JOHNS HOPKINS UNIVERSITY APPLIED PHYSICS LABORATORY (2/02 – 4/04)

Position: *Senior Professional Staff*

- Mars Reconnaissance Orbiter Spacecraft CRISM Instrument:
 - Designed IEEE Floating Point Multiply and Accumulate ACTEL RT54SX72A FPGA for Gimbal
 - Designed Imaging board ACTEL RT54SX72A FPGA for Focal Plane
 - Designed Video Processing Pipeline and Compression ACTEL RT54SX72A FPGA for Focal Plane Interface Card
 - Designed RTX2010 μ P Interface ACTEL RT54SX72A FPGA for Focal Plane Interface Card
- Messenger Spacecraft: Designed 8 Channel Concentrator Instrument Interface Board and ACTEL RT54SX72A FPGA
- Chebyshev Data Compression: Implemented Two Dimensional Chebyshev Compression in hardware ALTERA 10K100 FPGA

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THALES CORPORATION – AVIONICS DIVISION (5/00 – 2/02)

Position: *Hardware Design Engineer*

- Tactical System Display: Designed Altera Cyclone FPGAs to selectively simulate I/O interfaces and verify normal operations of the Processor-Thermal-Human Interface and Power Supply Modules
- Kiowa Warrior OH-58D ISMS (Integrated Storage Management System)
 - 20k Altera FPGA design for FEP (Front-End Processing) module. Included 1553 and PowerPC interfaces
 - Lattice FPGA design for the communication with Hell Fire Missiles
 - Lattice FPGA design for the Rocket Control Card Fusing and Firing sequences.

AAI CORPORATION (5/00 – 12/00)

Position: *Senior Design Engineer*

- FPGA designer for Northrup Grumman Doppler Radar System Trainer (Xilinx Virtex XCV300E)
- FPGA FIR filter implementation
- Xilinx Foundation, Synplicity Synplify and Active HDL.

Position: *Senior Design Engineer* (1/99 – 12/99)

- FPGA designer for Fire Control Radar (MK 95).
- DSP FIR Filter implementation
- Developed CW IF Generator, Xilinx 4028, 30k gate FPGA in VHDL.
- Xilinx Foundation Tool Set.

RAYTHEON COMMUNICATION SYSTEMS/ALLIED SIGNAL (4/98 – 12/98)

Position: *Senior Design Engineer*

- FPGA designer for MIDS secured communication system.
- Developed Receive Transmit Module, 50k gate FPGA in VHDL.
- Test bench with ModelSim and Synthesized with Synplicity Synplify.

HUGHES NETWORK SYSTEMS (12/97 - 4/98)

Position: *Senior Design Engineer*

- Designed parallel differential bus for IF distribution monitoring system.
- Developed and Implemented Design Verification Test Plan for ICO Satellite Communication System.
- Switching Transcoder Module with 12 TMS320C31 DSPs and Intel 960 microprocessor.

ADE OPTICAL SYSTEMS (8/97 - 12/97)

Position: *Senior Design Engineer*

- Developed and integrated VME board for silicon wafer scanning machine.
- Board consisted of TMS320C50, ALTERA 8000 FPGA, and 7000 EPLD devices.

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WATKINS JOHNSON CORPORATION (3/97 - 6/97)

Position: *Senior Design Engineer*

- 100 MHz, TDM Telecommunications Interpolation board for VME bus.
- FIR filter implementation
- Designed high speed ECL logic clock driving circuit.
- Designed and tested new JTAG protocol for ALTERA, EPLDs.
- ALTERA EPLD, AHDL, schematic capture design.

Position: *Hardware Design Engineer* (10/95 - 7/96)

- High Speed DSP synthesizer for cellular base station communications.
- Integrated DSP board with existing VME bus system.
- FIR filter design.
- ALTERA, FPGA and EPLD design.
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ARBITRON CORPORATION (7/96 - 3/97)

Position: *Senior Design Engineer*

- Designed TMS320C31 multiprocessor board for STD32 backplane.
- Developed bus protocol for multiple controllers and peripherals.
- High resolution A/D and D/A board for audio application.